REMARKS

This amendment responds to the office action mailed October 27, 2005. In the office action the Examiner:

- allowed claims 9-24;
- rejected claim 2 under 35 U.S.C. 112, second paragraph;
- rejected claims 2-4, 6 and 25 under 35 U.S.C. 103(a) as being unpatentable over Butler et al. (US 6,720,968) and Harriman (US 6,330,645);
- rejected claims 7 and 8 under 35 U.S.C. 103(a) as being unpatentable over Butler et al. (US 6,720,968) and Harriman (US 6,330,645) and Lo et al. (US 6,115,760);
- rejected claim 5 under 35 U.S.C. 103(a) as being unpatentable over Butler et al. (US 6,720,968) and Harriman (US 6,330,645) and Takada et al (US 6,633,961)

After entry of this amendment, the pending claims are: claims 2-25.

Overview of Changes to Claims

Claim 2 has been amended to address the 112, 2nd paragraph issue identified by the Examiner in the present Office Action. Claims 2 and 25 have been amended to clarify that the read and write commands are pipelined. Support is found in paragraph 18 of the specification for the present application. These amendments, therefore, do not constitute new matter.

35 USC 112, 2nd Paragraph Rejections

In the present Office Action, the Examiner has rejected claim 2 as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention. After entry of this reply, claim 2 has been amended to indicate "a data bus" instead of "the data bus." Removal of this ground for rejection is requested.

35 USC 103(a) Rejections

In the present Office Action, the Examiner has rejected claims 2-4, 6 and 25 as being unpatentable over Butler and Harriman. The Applicants disagree and traverse.

As discussed in col. 1, lines 41-67, Butler addresses problems associated with a finite buffer size and finite bandwidth in a video acquisition system as opposed to data "bubbles" in a pipelined memory as defined by pending independent claims 2 and 25. As a consequence,

in Butler "the arbitration logic determines if ***any*** write requests, refresh requests or read requests are pending" (col. 2, lines 44-46) as opposed to specific commands associated with a specific address, such as the claimed first address in independent claims 2 and 25. Butler, therefore, is addressed to a different problem than pending independent claims 2 and 25.

As discussed in the previous reply, and as noted by the Examiner in the present Office Action (pp. 2 and 3), the system in Harriman is designed to address coherency issues for multiple memory access streams issued by multiple memory controller access devices (abstract, lines 1-2). Harriman, therefore, does not address the pipeline data bubble problem that is addressed by the present invention as defined by the pending independent claims 2 and 25.

In the absence of a problem to be solved, there is no motivation to find a solution. Since Butler and Harriman are addressing different problems than the present invention, and since Butler explicitly indicates that arbitration is for any command (as opposed to specific commands associated with specific memory addresses), there is no motivation to combine the cited references (Butler and Harriman). The cited combination, therefore, is not *prima facie* obvious. Claims 2 and 25, and thus, dependent claims 3-4 and 6, are unobvious over the cited combination. Removal of this ground for rejection is requested.

In the present Office Action, the Examiner has rejected claims 7 and 8 as being unpatentable over Butler and Harriman and Lo et al. The Applicants disagree and traverse.

As argued above, there is no motivation to combine Butler and Harriman to achieve the limitations of claim 2, and thus, claims 7 and 8. Lo et al. addresses a scalable buffer for coupling between digital domains. Lo et al, therefore, does not teach or suggest a motivation for combining the cited references. The cited combination, therefore, is not *prima facie* obvious. Claims 7 and 8 are unobvious over the cited combination. Removal of this ground for rejection is requested.

In the present Office Action, the Examiner has rejected claim 5 as being unpatentable over Butler and Harriman and Takada et al. The Applicants disagree and traverse.

As argued above, there is no motivation to combine Butler and Harriman to achieve the limitations of claim 2, and thus, claim 5. Furthermore, Takada et al. does not teach or suggest such a motivation for combining the cited references. In fact, Takada et al. concerns

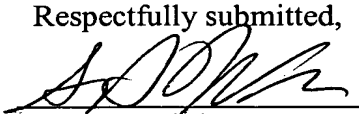
the insertion of data into a data stream on a transmission medium and does not teach writing data from a buffer to a memory device while a controller is idle. (The information written to memory in the text cited by the Examiner is actually link information, but the link information is not data stored in the buffers of Takada et al. Rather, the link information is produced by a controller and is used to control the order in which data is transferred from the buffers to the data stream on the transmission medium.) Takada et al. therefore does not address neither a problem nor a system architecture that is analogous to the problem and system architecture of claim 5. The cited combination, therefore, is not *prima facie* obvious. Claim 5 is unobvious over the cited combination. Removal of this ground for rejection is requested.

CONCLUSION

In light of the above amendments and remarks, the Applicant respectfully requests that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: January 27, 2006



31,066
(Reg. No.)

Gary S. Williams
MORGAN, LEWIS & BOCKIUS LLP
2 Palo Alto Square, Suite 700
3000 El Camino Real, Suite 700
Palo Alto, California 94306
(650) 843-4000